MC74AC74, MC74ACT74

Dual D-Type Positive Edge-Triggered Flip-Flop

The MC74AC74/74ACT74 is a dual D−type flip−flop with Asynchronous Clear and Set inputs and complementary (Q,$\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Outputs Source/Sink 24 mA
- ′ACT74 Has TTL Compatible Inputs
- Pb−Free Packages are Available

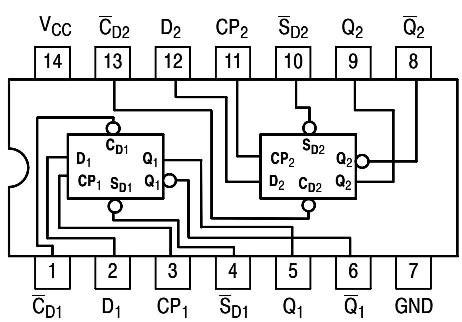


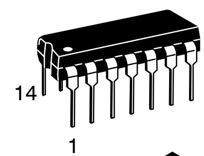
Figure 1. Pinout: 14−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

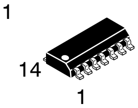
PIN	FUNCTION
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

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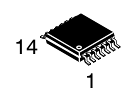
http://onsemi.com



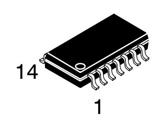
PDIP−14
N SUFFIX
CASE 646



SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DT SUFFIX
CASE 948G



SOEIAJ−14
M SUFFIX
CASE 965

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

October, 2006 − Rev. 7

Publication Order Number:
MC74AC74/D

TRUTH TABLE (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

NOTE: H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial;
↑ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

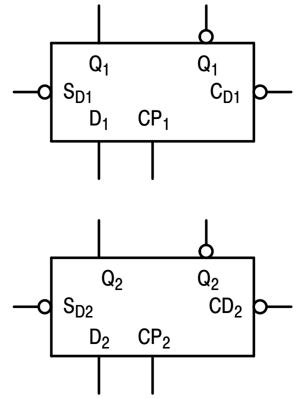
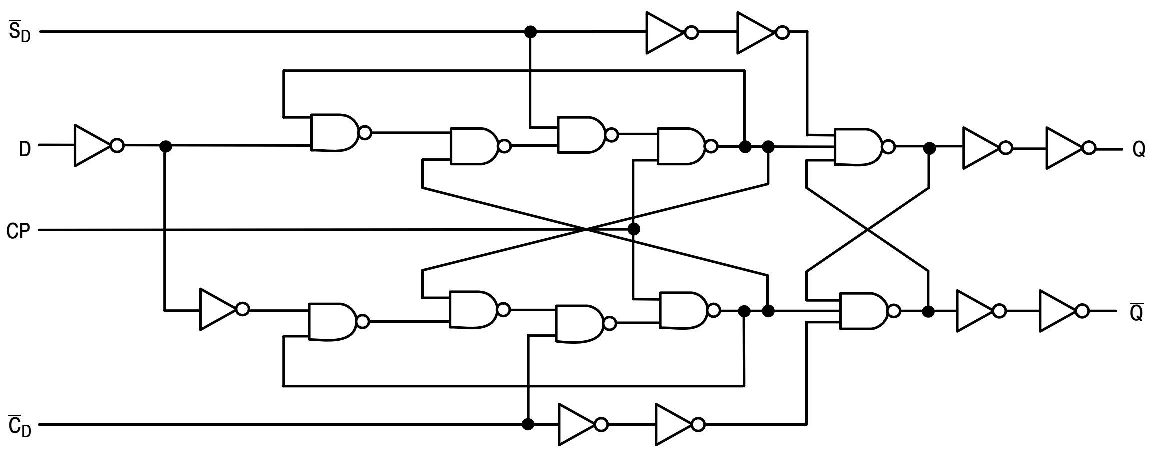


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – High		–	–	–24	mA
I_{OL}	Output Current – Low		–	–	24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC		74AC	Unit	Conditions
			T_A = +25°C		T_A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = –50 μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.
NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = −40°C$ to $+85°C$ $C_L = 50$ pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160	– –	95 125	– –	MHz	3–3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	5.0 3.5	8.0 6.0	12.5 9.0	4.0 3.0	13.0 10.0	ns	3–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	3.5 2.5	13.5 10.5	ns	3–6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	4.0 3.0	16.0 10.5	ns	3–6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	3.5 2.5	14.5 10.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		74AC $T_A = −40°C$ to $+85°C$ $C_L = 50$ pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW D_n to CP_n	3.3 5.0	1.5 1.0	4.0 3.0	4.5 3.0	ns	3–9
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3 5.0	−2.0 −1.5	0.5 0.5	0.5 0.5	ns	3–9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	7.0 5.0	ns	3–6
t_{rec}	Recovery TIme $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −2.0	0 0	0 0	ns	3–9

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C Typ	74ACT T_A = +25°C Guaranteed Limits	74ACT T_A = −40°C to +85°C Guaranteed Limits	Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 µA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	µA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	µA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210	–	125	–	MHz	3–3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	5.5	9.5	2.5	10.5	ns	3–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	3.0	11.5	ns	3–6
t_{PLH}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	5.0	4.0	7.5	11.0	4.0	13.0	ns	3–6
t_{PHL}	Propagation Delay C_{Pn} to Q_n or $\overline{Q}_n$	5.0	3.5	6.0	10.0	3.0	11.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	3.5	ns	3–9
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	–0.5	1.0	1.0	ns	3–9
t_w	C_{Pn} or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.0	ns	3–6
t_{rec}	Recovery TIme $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	–2.5	0	0	ns	3–9

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

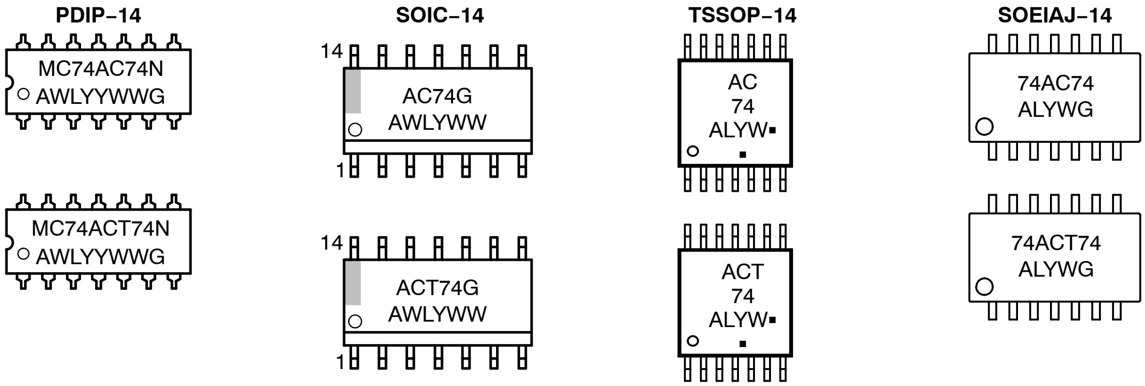
Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0 V

ORDERING INFORMATION

Device	Package	Shipping†
MC74AC74N	PDIP−14	25 Units/Rail
MC74AC74NG	PDIP−14 (Pb−Free)	
MC74ACT74N	PDIP−14	
MC74ACT74NG	PDIP−14 (Pb−Free)	
MC74AC74D	SOIC−14	55 Units/Rail
MC74AC74DG	SOIC−14 (Pb−Free)	
MC74AC74DR2	SOIC−14	2500/Tape & Reel
MC74AC74DR2G	SOIC−14 (Pb−Free)	
MC74ACT74D	SOIC−14	55 Units/Rail
MC74ACT74DG	SOIC−14 (Pb−Free)	
MC74ACT74DR2	SOIC−14	2500/Tape & Reel
MC74ACT74DR2G	SOIC−14 (Pb−Free)	
MC74AC74DT	TSSOP−14*	96 Units/Rail
MC74AC74DTR2	TSSOP−14*	2500/Tape & Reel
MC74AC74DTR2G	TSSOP−14*	
MC74ACT74DT	TSSOP−14*	96 Units/Rail
MC74ACT74DTR2	TSSOP−14*	2500/Tape & Reel
MC74ACT74DTR2G	TSSOP−14*	
MC74AC74MEL	SOEIAJ−14	2000/Tape & Reel
MC74AC74MELG	SOEIAJ−14 (Pb−Free)	
MC74ACT74MEL	SOEIAJ−14	
MC74ACT74MELG	SOEIAJ−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MARKING DIAGRAMS

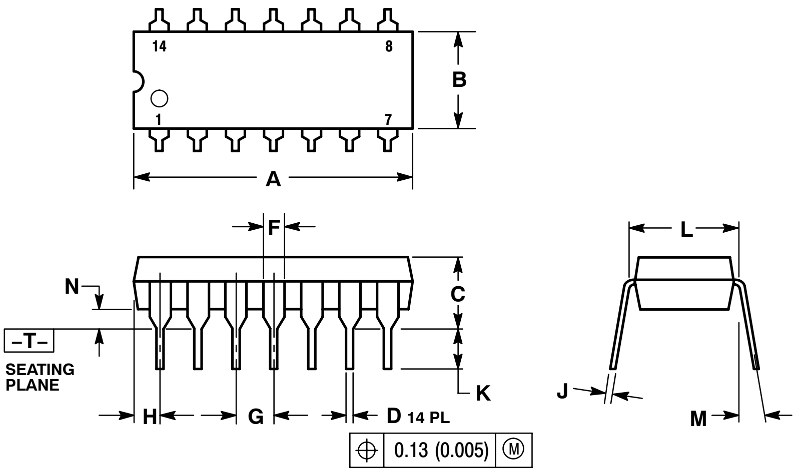


A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

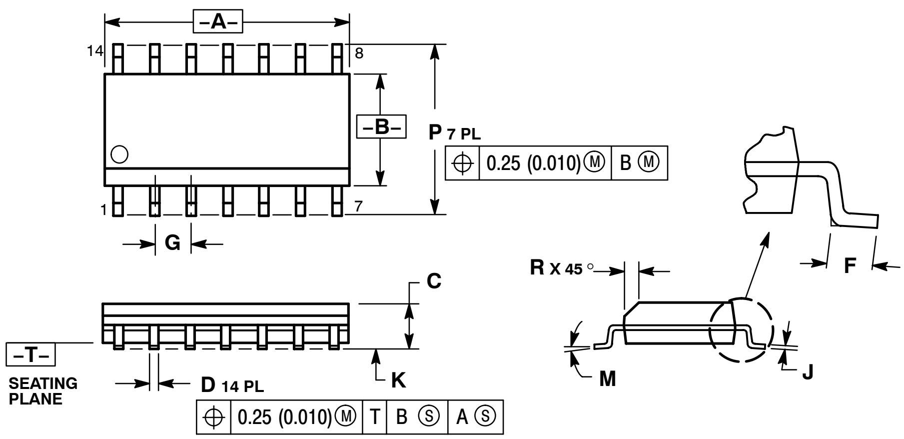
PDIP−14
CASE 646−06
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10°	−−−	10°
N	0.015	0.039	0.38	1.01

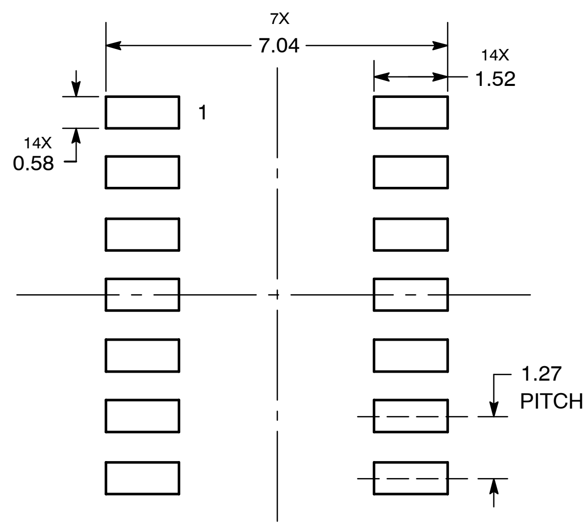
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

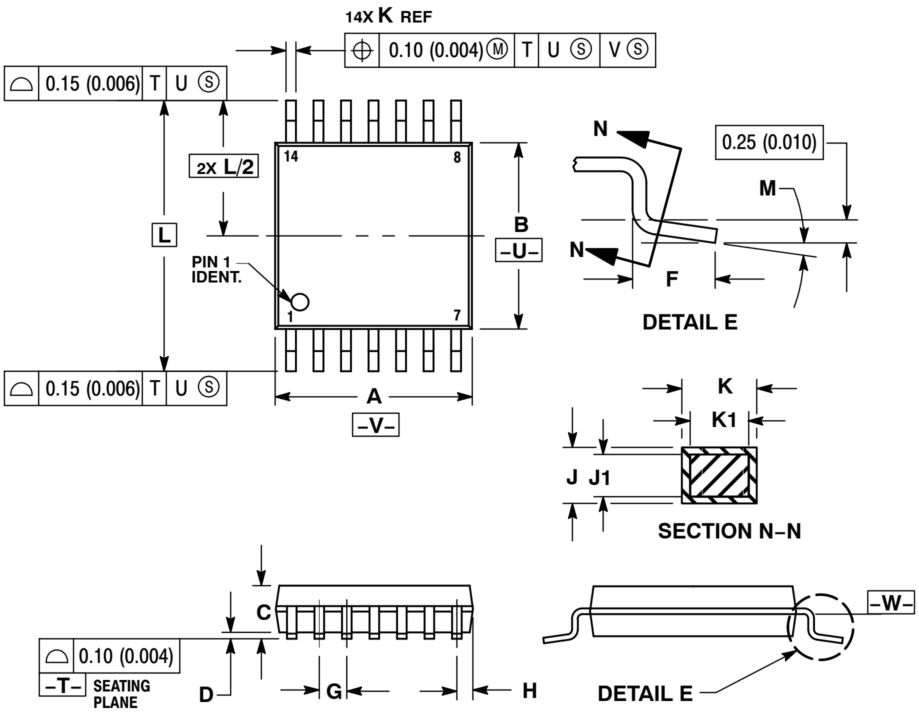
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

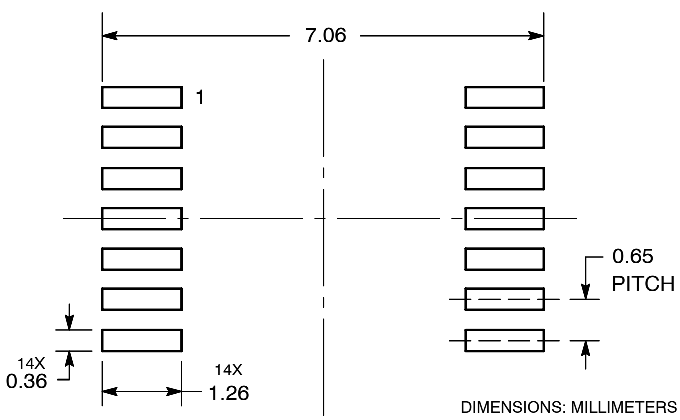
TSSOP−14
CASE 948G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

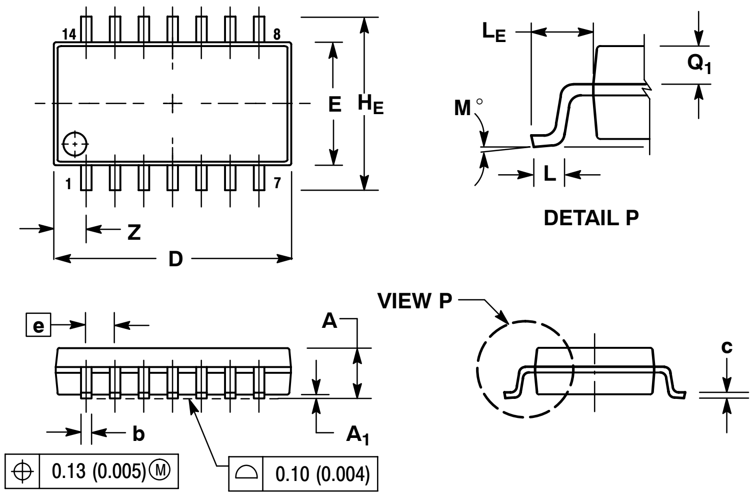
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOEIAJ−14
CASE 965−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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